

SN54ABTH16460, SN74ABTH16460 4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS207F – OCTOBER 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABTH16460 are 4-bit to 1-bit multiplexed registered transceivers used in applications where four separate data paths must be multiplexed onto or demultiplexed from a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. These devices also are useful in memory-interleaving applications.

Five 4-bit I/O ports ($1A-4A$, $1B1-4$, $2B1-4$, $3B1-4$, and $4B1-4$) are available for address and/or data transfer. The output-enable ($\overline{OEB}$, $\overline{OEB1}-\overline{OEB4}$, and $\overline{OEA}$) inputs control the bus-transceiver functions. These control signals also allow 4-bit or 16-bit control, depending on the $\overline{OEB}$ level.

SN54ABTH16460 . . . WD PACKAGE
SN74ABTH16460 . . . DGG OR DL PACKAGE
(TOP VIEW)

LEAB1	1	56	$\overline{OEB1}$
LEAB2	2	55	$\overline{OEB2}$
LEBA	3	54	SEL0
GND	4	53	GND
LEB1	5	52	1B1
LEB2	6	51	1B2
V_{CC}	7	50	V_{CC}
CLKBA	8	49	1B3
$\overline{OEB}$	9	48	1B4
CLKAB	10	47	2B1
GND	11	46	GND
1A	12	45	2B2
2A	13	44	2B3
CE_SEL0	14	43	2B4
CE_SEL1	15	42	3B1
3A	16	41	3B2
4A	17	40	3B3
GND	18	39	GND
CLKENAB	19	38	3B4
CLKENB	20	37	4B1
CLKENBA	21	36	4B2
V_{CC}	22	35	V_{CC}
LEB3	23	34	4B3
LEB4	24	33	4B4
GND	25	32	GND
$\overline{OEA}$	26	31	SEL1
LEAB3	27	30	$\overline{OEB3}$
LEAB4	28	29	$\overline{OEB4}$



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SN54ABTH16460, SN74ABTH16460

4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

Address and/or data information can be stored using the internal storage latches/flip-flops. The latch-enable (LEB1–LEB4, LEBA, and LEAB1–LEAB4) and clock/clock-enable (CLK/CLKEN) inputs are used to control data storage. When either one of the latch-enable inputs is high, the latch is transparent (clock is a don't care as long as the latch enable is high). When the latch-enable input goes low (providing that the clock does not transit from low to high), the data present at the inputs is latched and remains latched until the latch-enable input is returned high. When the clock enable is low and the corresponding latch enable is low, data can be clocked on the low-to-high transition of the clock. When either the clock enable or the corresponding latch enable is high, the clock is a don't care.

Four select pins (SEL0, SEL1, CE_SEL0, and CE_SEL1) are provided to multiplex data (A port), or to select one of four clock enables (B port). This allows the user the flexibility of controlling one bit at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH16460 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH16460 is characterized for operation from -40°C to 85°C .

Function Tables

A-TO-B OUTPUT ENABLE[†]

INPUTS		OUTPUT Bn
$\overline{OEB}$	$\overline{OEBn}$	
H	H	Z
H	L	Z
L	H	Z
L	L	Active

[†] n = 1, 2, 3, 4

A-TO-B STORAGE
(assuming $\overline{OEB} = \text{L}$, $\overline{OEBn} = \text{L}$)[‡]

INPUTS								OUTPUTS			
CLKENAB	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A ₀	A ₀	A ₀
X	X	X	H or L	H	H	H	L	A	A	A	A ₀
L	X	X	L	L	L	L	L	A ₀	A ₀	A ₀	A ₀
L	L	L	↑	L	L	L	L	A	A ₀	A ₀	A ₀
L	L	H	↑	L	L	L	L	A ₀	A	A ₀	A ₀
L	H	L	↑	L	L	L	L	A ₀	A ₀	A	A ₀
L	H	H	↑	L	L	L	L	A ₀	A ₀	A ₀	A
H	X	X	↑	L	L	L	L	A ₀	A ₀	A ₀	A ₀

[‡] This table does not cover all the latch-enable cases since they have similar results.



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Function Tables (Continued)

B-TO-A STORAGE
(before point P)

INPUTS								P
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	
X	X	H	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	H	B4
L ↑ L L L L						L	L	B1
						L	H	B2
						H	L	B3
						H	H	B4
L L L L L L						L	L	B1 [†]
						L	H	B2 [†]
						H	L	B3 [†]
						H	H	B4 [†]

[†] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE
(after point P)

INPUTS					OUTPUT A
CLKENBA	CLKBA	LEBA	OE $\overline{\text{A}}$	B	
X	X	X	H	X	Z
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A ₀ [†]
L	↑	L	L	L	L
L	↑	L	L	H	H
L	L	L	L	X	A ₀ [†]

[†] Output level before the indicated steady-state input conditions were established

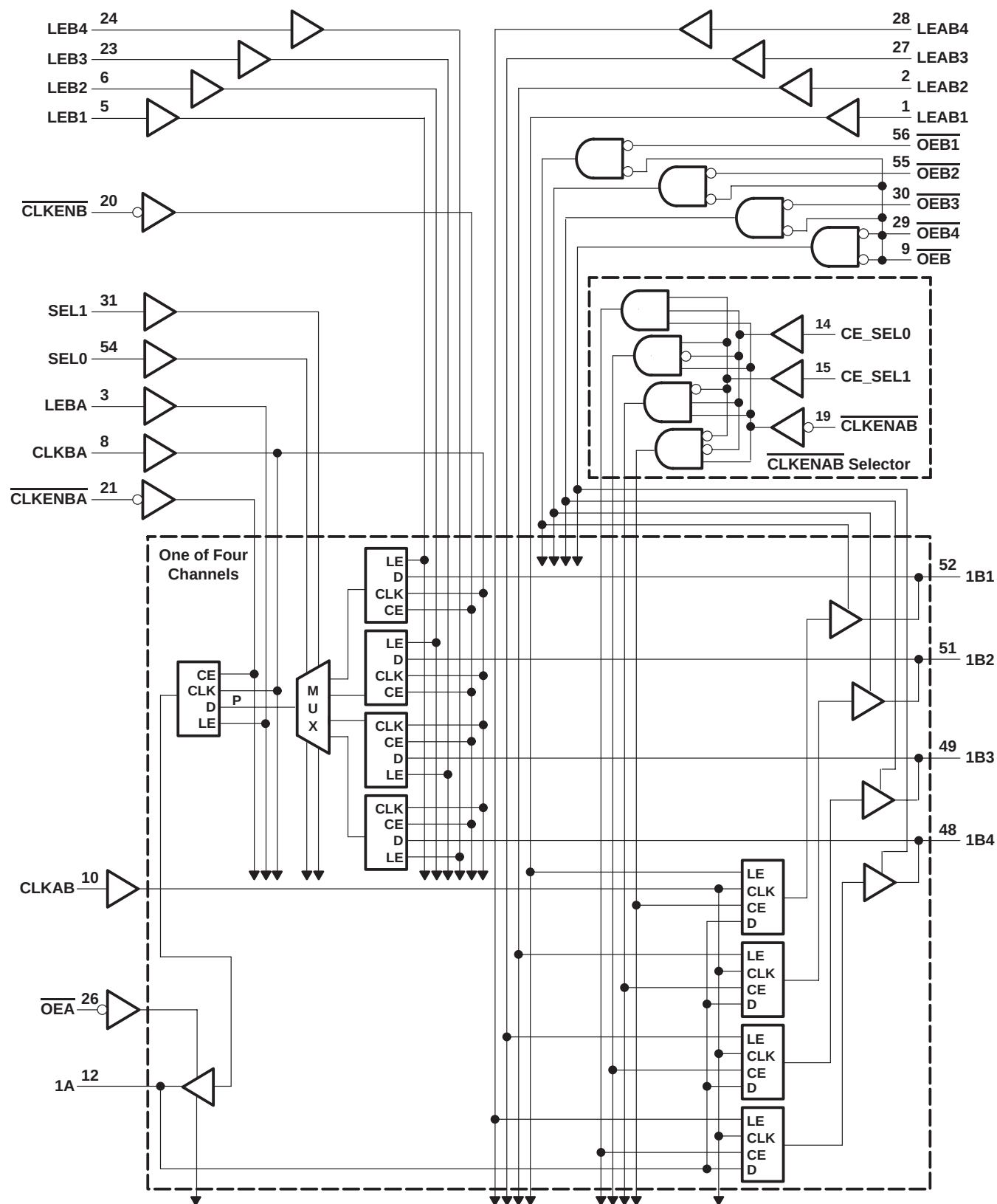
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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH16460	96 mA
SN74ABTH16460	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTH16460		SN74ABTH16460		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABTH16460		SN74ABTH16460		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2		−1.2		V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = −3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = −3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = −24 mA	2			2				
			I _{OH} = −32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 48 mA	0.36			0.5				V
			I _{OL} = 64 mA	0.55*					0.55		
V _{hys}				100							mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20			±20		±20		
I _I (hold)	A or B ports	V _{CC} = 4.5 V	V _I = 0.8 V	75	500	75	500	75	500	μA	
			V _I = 2 V	−75	−500	−75	−500	−75	−500		
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X		±50			±50		±50		μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X		±50			±50		±50		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O §		V _{CC} = 5.5 V,	V _O = 2.5 V	−50	−100	−200	−50	−200	−50	−200	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	1.5			1.5		1.5		mA
			A outputs low	10			10		10		
			B outputs low	32			32		32		
			Outputs disabled	1.5			1.5		1.5		
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5		mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		8							pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		3.5							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54ABTH16460		SN74ABTH16460		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	160	0	160	MHz
t_w	Pulse duration	CLKAB high or low	3.8		3.8		ns
		CLKBA high or low	4.5		4.5		
		LEAB1, 2, 3, or 4 high	2.2		2.2		
		LEBA high	2.1		2.1		
		LEB1, 2, 3, or 4 high	2.4		2.4		
t_{su}	Setup time	Before CLKAB $\uparrow$	A bus	2.5	2.5		ns
			CE_SEL0/1	3.2	3.2		
			CLKENAB	3.2	3.2		
		Before LEAB1, 2, 3, or 4 $\downarrow$	A bus	3.6	3.6		
			B bus	3.8	3.8		
			CLKENB	2.3	2.3		
		Before CLKBA $\uparrow$	CLKENBA	2.5	2.5		
			LEB1, 2, 3, or 4	4.3	4.3		
			SEL0/1	4.5	4.5		
		Before LEB1, 2, 3, or 4 $\downarrow$	B bus	3.2	3.2		
			B bus	4	4		
			LEB1, 2, 3, or 4	4.4	4.4		
t_h	Hold time	After CLKAB $\uparrow$	A bus	0.5	0.5		ns
			CE_SEL0/1	1.1	1.1		
			CLKENAB	0.5	0.5		
		After LEAB1, 2, 3, or 4 $\downarrow$	A bus	1.2	1.2		
			B bus	1.3	1.3		
			CLKENB	1	1		
		After CLKBA $\uparrow$	CLKENBA	1	1		
			SEL0/1	0	0		
		After LEB1, 2, 3, or 4 $\downarrow$	B bus	1.5	1.5		
			B bus	0.4	0.4		
			SEL0/1	0.1	0.1		

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4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABTH16460		SN74ABTH16460		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			160			160		160		MHz
t_{PLH}	B	A	2.5	3.6	5.9	2.5	7.1	2.5	6.5	ns
t_{PHL}			2	3.5	5.8	2	6.8	2	6.5	
t_{PZH}	$\overline{\text{OEA}}$	A	1.5	2.8	4.8	1.5	5.9	1.5	5.6	ns
t_{PZL}			1.5	2.6	4.6	1.5	5.5	1.5	5.2	
t_{PHZ}	$\overline{\text{OEA}}$	A	2.5	3.8	5.3	2.5	6	2.5	5.9	ns
t_{PLZ}			1.5	4.6	6.1	1.5	7	1.5	6.5	
t_{PLH}	A	B	2	3.2	5.2	2	6.2	2	5.7	ns
t_{PHL}			1.5	3.1	5.2	1.5	6.1	1.5	5.7	
t_{PZH}	$\overline{\text{OEB}}$	B	1.5	3.3	5.7	1.5	6.7	1.5	6.4	ns
t_{PZL}			1.5	3.2	5.5	1.5	6.6	1.5	6.3	
t_{PHZ}	$\overline{\text{OEB}}$	B	3	4.7	6.3	3	7.1	3	7	ns
t_{PLZ}			2	4	5.5	2	6.6	2	6.1	
t_{PZH}	$\overline{\text{OEB1}}, \overline{2}, \overline{3}, \overline{4}$	B	1.5	3	5.2	1.5	6	1.5	5.8	ns
t_{PZL}			1.5	2.9	4.9	1.5	5.9	1.5	5.6	
t_{PHZ}	$\overline{\text{OEB1}}, \overline{2}, \overline{3}, \overline{4}$	B	2.5	4	5.7	2.5	6.2	2.5	6.1	ns
t_{PLZ}			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
t_{PLH}	CLKBA	A	1.5	4.2	6.7	1.5	8.1	1.5	7.4	ns
t_{PHL}			1.5	4.4	6.9	1.5	8.4	1.5	7.7	
t_{PLH}	CLKAB	B	2	3.4	5.6	2	6.8	2	6.2	ns
t_{PHL}			2	3.4	5.3	2	6.3	2	5.9	
t_{PLH}	LEBA	A	2	3	5	2	6.1	2	5.6	ns
t_{PHL}			2	3.1	4.8	2	5.8	2	5.3	
t_{PLH}	LEAB1, 2, 3, 4	B	2	3.2	5.2	2	6.3	2	5.8	ns
t_{PHL}			2	3.3	5	2	6.1	2	5.6	
t_{PLH}	LEBA1, 2, 3, 4	A	2.5	4	6.5	2.5	7.8	2.5	7.2	ns
t_{PHL}			2.5	4	6.1	2.5	7.5	2.5	6.8	
t_{PLH}	SEL	A	2	4.1	6.7	2	8.1	2	7.5	ns
t_{PHL}			2	3.8	6.2	2	7.3	2	6.9	

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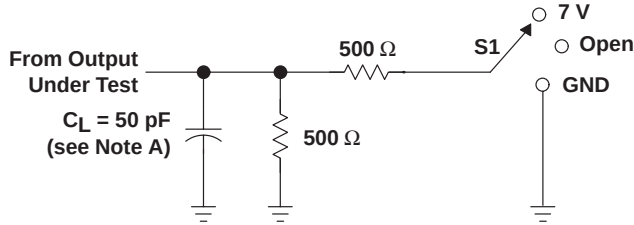


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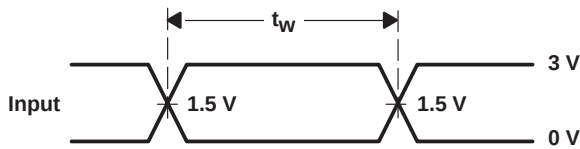
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PARAMETER MEASUREMENT INFORMATION

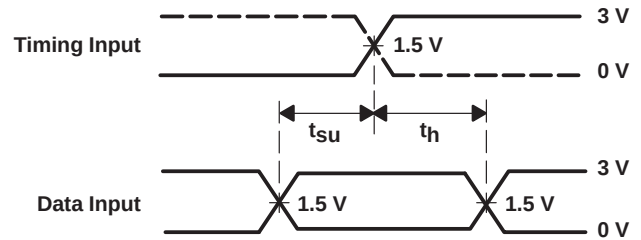


LOAD CIRCUIT

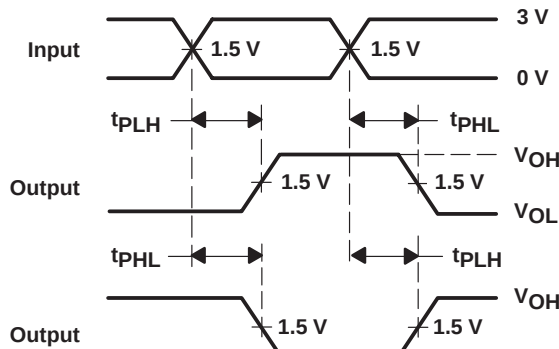
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



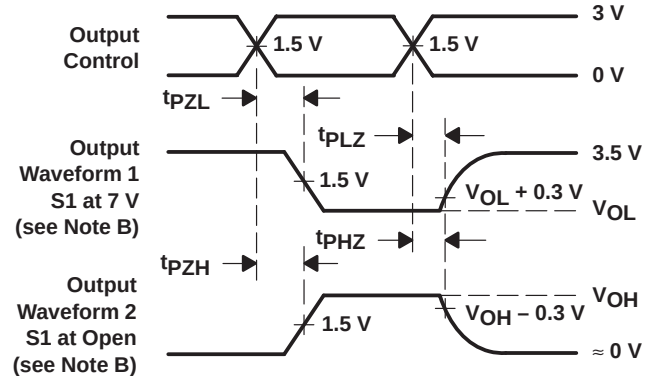
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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